## REMARKS

Applicant appreciates the detailed examination evidenced by the Office Action mailed May 11, 2004 (hereinafter the Office Action). Applicant has amended Claim 13 to correct a typographical error. Applicant submits that the pending claims are patentable over the cited references for the reasons provided below.

**Claims 1-14 Are Patentable Over Nakamura**

Claims 1-14 have been rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,555,481 to Nakamura (hereinafter "Nakamura").

Independent Claim 1 recites (emphasis added):

> 1. An integrated circuit memory device comprising:
> a semiconductor substrate;
> a plurality of word line structures on predetermined portions of the semiconductor substrate;
> word line contact plugs, each of which is disposed between adjacent word line structures;
> storage node contact plugs in electrical contact with predetermined ones of the word line contact plugs;
> storage node electrodes on the storage node contact plugs; and
> a plate electrode between the storage node electrodes and between the storage node contact plugs.

Accordingly, storage node contact plugs are in electrical contact with word line contact plugs, storage node electrodes are on the storage node contact plugs, and the plate electrode is between the storage node electrodes and between the storage node contact plugs. In rejecting Claim 1, the Office Action states on page 2 that Nakamura discloses "storage node contact plugs 11 in electrical contact with predetermined ones of the [word line] WL contact plugs; storage node electrodes 16 on the storage node contact plugs; and plate electrodes 18 between the storage node electrodes and between the storage node contact plugs." However, this interpretation of Nakamura by the Office Action appears to be contrary to the referenced figures and express teachings of Nakamura.

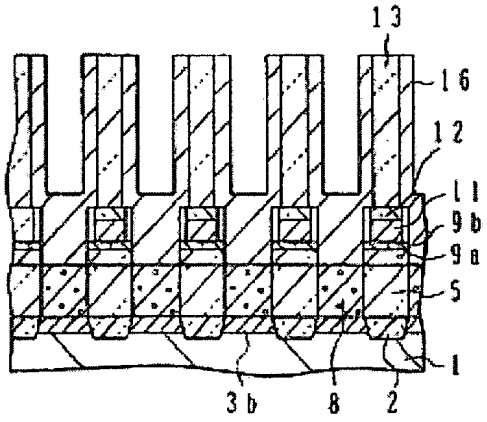
Initially, Applicant notes that Nakamura consistently refers to element 11 as a "bit line", not as a storage node contact plug as contended by the Office Action. Indeed, Nakamura does not appear to disclose or suggest storage node contact plugs in electrical contact with predetermined ones of word line contact plugs, and storage node electrodes on the storage node contact plugs.

Moreover, even if, for the sake of this analysis only, the bit line 11 is interpreted as a "storage node contact plug", Nakamura would still fail to disclose a plate electrode that is between the storage node contact plugs. Nakamura discloses the following process for forming the storage electrode 16:

> In succession, the silicon oxide film 9a is etched to expose the upper surface of the storage electrode lower plug 8.
> As shown in FIGS. 18A to 18D, a storage electrode film is formed over the whole substrate surface. ... In this case, the opening above the storage electrode lower plug 8 is buried with the storage electrode film. The storage electrode film deposited on the upper surface of the insulating layer 13 is removed by CMP or the like to leave a storage electrode 16.

(Nakamura, Col. 10, lines 49-59, emphasis added). Accordingly, Nakamura discloses that the "opening above the storage electrode lower plug 8 is buried with the storage electrode film", so that the storage electrode 16 fills the gap between the "storage node contact plug" 11, as shown in FIG. 18D below.

FIG.18D




Nakamura then discloses that "[as] shown in FIGS. 19A to 19D, after a capacitor dielectric film 17 is formed over the whole substrate surface, covering the

storage electrode 16, a plate electrode 18 is formed on the capacitor dielectric film 17." Accordingly, as shown in FIGS. 19A to 19D below, because a gap is not left between the "storage node contact plug" 11, and is instead filled with the storage electrode 16, the plate electrode 18 is not between the "storage node contact plug" 11.

FIG. 19A

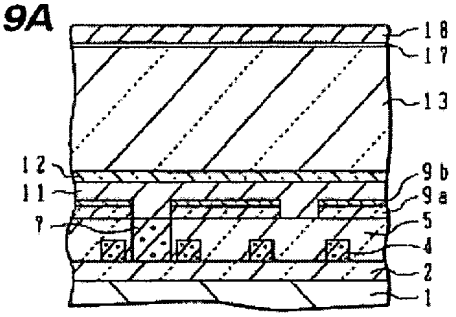



FIG. 19B

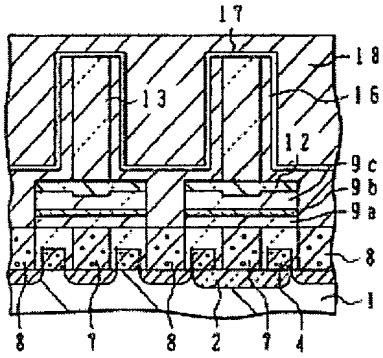



FIG. 19C

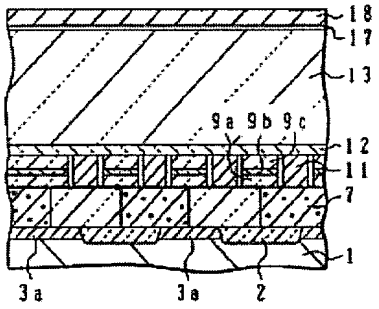
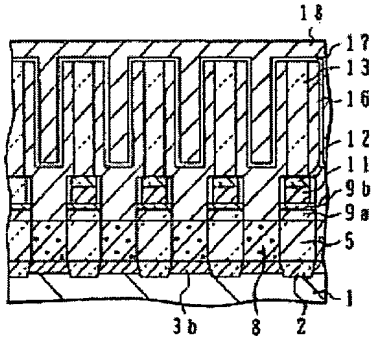



FIG. 19D




In sharp contrast to Nakamura, the embodiment of the present invention shown in FIGs. 2C and 2D below leaves a gap between the storage node contact plugs 124, which is later filled with the plate electrode 132 so that the plate electrode 132 is between the storage node electrodes 126 and between the storage node contact plugs 124.

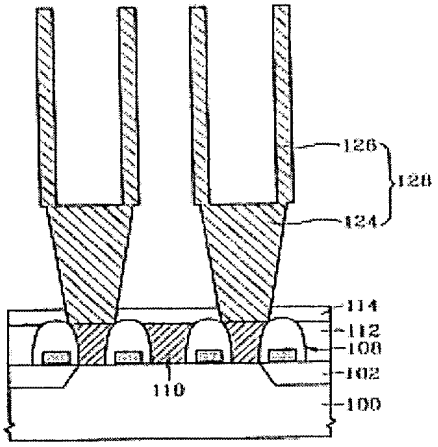



*FIG. 2C*

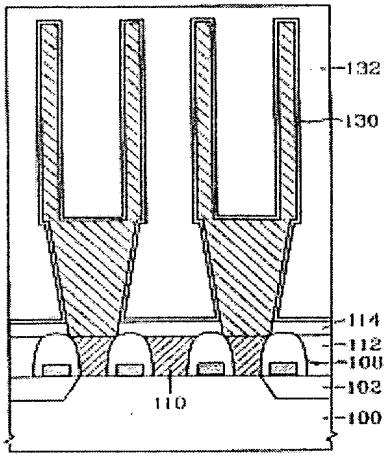



*FIG. 2D*

For at least these reasons, Applicant respectfully submits that Nakamura fails to disclose each and every element of Claim 1, and therefore that Claim 1 is patentable over Nakamura.

Independent Claim 8 recites, among other things, "a plate electrode on the dielectric layer and between the storage node contact plugs and between the storage node electrodes." Accordingly, Claim 8 is patentable over Nakamura for substantially the same reasons as explained for Claim 1.

Dependent Claims 2-5 and Claims 9-14 are patentable as depending respectively from allowable independent Claims 1 and 8. Moreover, these claims provide further bases for patentability. For example, Claims 2 and 9 recite that the plate electrode extends between lower portions of the storage node contact plugs, which is not disclosed by Nakamura. Applicant notes that the Office Action fails to disclose where Nakamura discloses the recitations of either of Claims 10 or 11, and indeed Applicant respectfully submits that Nakamura fails to disclose Claims 10 and 11. In rejecting Claim 12, the Office Action contends that Nakamura discloses that "storage node electrodes are directly on the storage node contact plugs". However,

the Office Action has referred to element 11 as a "storage node electrode", which is shown in the figures (see FIGS. 19A-D) as not being "directly on the storage node contact plugs."

Independent Claim 6 recites (emphasis added):

> 6. An integrated circuit memory device, comprising:
> a semiconductor substrate;
> a pair of spaced apart word line structures on the substrate;
> an interlayer insulating layer on the word line structures;
> a bit line structure on the interlayer insulating layer that is transverse to the word line structures;
> a first capacitor electrode that extends from the substrate between adjacent word line structures, through the interlayer insulation layer, and beyond the bit line structure;
> a capacitor dielectric on the first capacitor electrode and directly on the bit line structure; and
> a second capacitor electrode on the capacitor dielectric.

Accordingly, Claim 6 recites that the capacitor dielectric is directly on the bit line structure, and the second capacitor electrode in on the capacitor dielectric. In rejecting Claim 6, the Office Action contends that Nakamura discloses "a capacitor dielectric 17 on the first capacitor electrode and directly on the BL structures", where the first capacitor electrode is referred to as element 16 and the BL structure is referred to as element 11. However, this contention is not supported by the disclosure of Nakamura, which shows in FIGs. 19A-D that the capacitor dielectric 17 is not directly on the bit line 11. Instead, FIGs. 19A and 19C shows intervening elements 13 and 12, and FIG. 19D shows intervening elements 16 and 12.

For at least these reasons, Applicant respectfully submits that Claim 6 is patentable over Nakamura.

Claim 7 is patentable as depending from allowable Independent Claim 6.

## CONCLUSION

In light of the above amendments and remarks, Applicant respectfully submits that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 29, 2004.

Audra Wooten